In re Patent Application of:
ENRIQUEZ ET AL
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In the Claims:

1. - 35. (Canceled)

36. (New) A subscriber line interface circuit comprising:

a high voltage analog section, containing analog operational circuits, operational parameters of which are programmable in accordance with respective bias currents supplied thereto, and to which power sufficient for any signaling conditions of tip and ring conductors of a respective subscriber loop pair is supplied, and being operative to drive said tip and ring conductors of said respective subscriber loop pair in accordance with analog input and analog control signals supplied thereto; and

a low voltage digitally programmable signal generation and digital signal processing section, that is operative to interface voice and ringing signals with said analog circuits of said high voltage analog section and to monitor and control operational characteristics of said analog circuits of said high voltage section, said low voltage digitally programmable signal generation and digital signal processing section including

a digital signal processor (DSP)-based codec, that is operative to interface said voice and ancillary signals, including low voltage signaling and ringing signals with said analog circuits of said high voltage analog section; and

a supervisory digital signal processor, separate from said codec, that is operative to program respective values of bias currents that control operational parameters of respective ones of said analog operational circuits, said bias currents as programmed by said supervisory digital signal processor being coupled to said analog operational circuits and thereby establishing said programmable operational parameters thereof.

37. (New) The subscriber line interface circuit according to

claim 36, wherein said high voltage section includes a control and latch interface unit that is operative to receive and store from said supervisory digital signal processor a plurality of digital input signals for defining values of said bias currents through which said operational parameters of said respective ones of said analog operational circuits of said high voltage section are established.

38. (New) The subscriber line interface circuit according to claim 36, wherein said high voltage section includes an input signal receiving unit, that is operative to interface and condition said voice and ancillary signals as supplied from said (DSP)-based codec of said low voltage digitally programmable signal generation and digital signal processing section.

39. (New) The subscriber line interface circuit according to claim 38, wherein said input signal receiving unit includes a voice signal path containing a voltage-sense, current-feed circuit to which voice signals are coupled from said CODEC, and a tip/ring amplifier unit, having respective tip and ring amplifier sections to which complementary polarity currents representative of voice signal signals are coupled from said voltage-sense, current-feed circuit, and having tip and ring outputs thereof adapted to be coupled to said tip and ring conductors of said respective subscriber loop pair.

40. (New) The subscriber line interface circuit according to claim 39, wherein each of said tip and ring amplifier sections of said tip/ring amplifier unit is configured for multiple mode operation, and having respectively different gain characteristics which are programmable in accordance with the intended mode of operation of said subscriber line interface circuit, as controlled by said supervisory digital signal processor.

41. (New) The subscriber line interface circuit according to claim 40, wherein said input signal receiving unit includes respective ancillary tip and ring signal paths containing respective tip and ring associated voltage-sense, current-feed circuits to which ancillary tip and ring signals are coupled from said CODEC.

42. (New) The subscriber line interface circuit according to claim 41, wherein each of said tip and ring amplifier sections of said tip/ring amplifier unit is configured to operate, under control of supervisory digital signal processor, at a first gain for voice signal transmission mode, and at a substantially increased second gain relative to said first gain for ancillary signal transmission mode.

43. (New) The subscriber line interface circuit according to claim 42, wherein each of said tip and ring amplifier sections contains a plurality of front end transconductance circuits coupled to a shared operational amplifier gain section, and having feedback resistors coupled from an output of said gain section to inputs of respective ones of said plurality of front end transconductance circuits, that define respectively different gain characteristics with input resistors associated with drive signal currents from said input signal receiving unit as defined by signals from said supervisory digital signal processor.

44. (New) The subscriber line interface circuit according to claim 43, wherein said plurality of front end transconductance circuits include a first front end transconductance circuit having a first valued feedback resistor coupled from said output of said gain section to a signal input of said first front end transconductance circuit, and a second front end transconductance circuit having a second valued feedback resistor, different from said first valued feedback resistor, and coupled from said output

of said gain section to a signal input of said second front end transconductance circuit, and wherein said signal input of said first front end transconductance circuit is arranged to receive a selected one of said voice signals and low voltage ancillary signals, and wherein said signal input of said second front end transconductance circuit is arranged to receive a low voltage ringing signal.

45. (New) The subscriber line interface circuit according to claim 44, wherein said first front end transconductance circuit is coupled to receive one of voice signals and low voltage signals, and said second front end transconductance circuit is coupled to receive ringing signals.

46. (New) The subscriber line interface circuit according to claim 40, wherein said high voltage analog section further includes a battery bias unit coupled to selectively couple prescribed bias voltages to voltage reference inputs of said tip and ring amplifier sections of said tip/ring amplifier unit in accordance with the mode of operation of said subscriber line interface circuit.

47. (New) The subscriber line interface circuit according to claim 46, wherein said battery bias unit is coupled to a battery supply switch unit that is operative to provide for the selection from among a plurality of different battery voltages.

48. (New) The subscriber line interface circuit according to claim 47, wherein said battery bias unit contains a set of switchable voltage divider networks coupled between said voltage reference inputs of said tip and ring amplifier sections of said tip/ring amplifier unit, and wherein said battery supply switch unit is operative to selectively couple either a high battery voltage VBH or a low battery voltage VBL to said battery bias unit.

49. (New) The subscriber line interface circuit according to claim 48, further including a battery monitor unit coupled to provide said supervisory digital signal processor with an indication of the battery voltage being selectively coupled by said battery supply switch unit.

50. (New) The subscriber line interface circuit according to claim 40, further including a sense amplifier coupled to outputs of said tip and ring amplifier sections of said tip/ring amplifier unit, and being operative to provide a voice signal summation for differential mode voice signals, and mutual cancellation of common mode signals.

51. (New) The subscriber line interface circuit according to claim 50, wherein an output of said sense amplifier is adapted to be coupled through an auxiliary amplifier to an analog feedback monitor port for closing a loop to synthesize the output impedance of said subscriber line interface circuit.

52. (New) The subscriber line interface circuit according to claim 50, wherein said sense amplifier comprises tip and ring associated voltage detectors, complementary-polarity coupled across tip and ring sense resistors at outputs of said tip and ring amplifier sections of said tip/ring amplifier unit.

53. (New) The subscriber line interface circuit according to claim 40, wherein said tip and ring amplifier sections of said tip/ring amplifier unit are coupled to respective tip and ring path loop detectors, that provide outputs representative of sensed tip and ring currents for application to said supervisory digital signal processor.

54. (New) The subscriber line interface circuit according to claim 40, wherein said tip and ring amplifier sections of said tip/ring amplifier unit are operative to controllably limit transient current therein.

55. (New) The subscriber line interface circuit according to claim 36, wherein said high voltage analog section includes a tip/ring amplifier unit having tip and ring outputs that are adapted to be coupled to respective ones of said tip and ring conductors of said respective subscriber loop pair, and having gain characteristics which are programmable in accordance with the intended mode of operation of said subscriber line interface circuit, as controlled by said programming signals supplied by said supervisory digital signal processor.

56. (New) The subscriber line interface circuit according to claim 55, wherein said input signal receiving unit includes respective ancillary tip and ring paths containing respective tip and ring associated voltage-sense, current-feed circuits, to which ancillary tip and ring control voltages are supplied, so as to place said tip/ring amplifier unit at respectively different gains in association with respectively different modes of operation of said subscriber line interface circuit.

57. (New) The subscriber line interface circuit according to claim 56, wherein said respective ancillary tip and ring paths and said tip/ring amplifier unit are configured to place said tip/ring amplifier unit at said respectively different gains in association with respectively different on-hook and off-hook modes of operation of said subscriber line interface circuit.

58. (New) The subscriber line interface circuit according to claim 36, wherein said tip/ring amplifier is coupled to controllably supply said tip and ring conductors with

respectively different sets of DC voltages, in accordance with the intended mode of operation of said subscriber line interface circuit, as programmed by said supervisory digital signal processor.